INTERNATIONAL UNIVERSITY LIAISON INDONESIA IULI

SYLLABUS

Date/ Revision 3 January 2017
Faculty Engineering
Approval

SUBJECT : Digital Logic & Digital Systems

1. Identification of Subject:

Name of Subject : Digital Logic & Digital Systems
Code of Subject :
SKS / ECTS :
Semester : Semester 3
Study Program : B-CSE
Lecturer :

2. Competency

After studying the course, the student will

- Understand the principles and methodology of digital logic design at the gate and switch level, including both combinational and sequential logic elements.
- Gain experience developing a relatively large and complex digital system.
- Gain experience with modern computer-aided design tools for digital logic design.
- Understand clocking methodologies used to control the flow of information and manage circuit state.
- Appreciate methods for specifying digital logic, as well as the process by which a high-level specification of a circuit is synthesized into logic networks.
- Appreciate the tradeoffs between hardware and software implementations of a given function.
- Appreciate the uses and capabilities of a modern FPGA platform.

3. Description of Subject:

This is a junior-level course in the computer science curriculum for digital system design and implementation. The course will cover design of synchronous digital systems using modern tools and methodologies, in particular, digital logic synthesis tools, digital hardware simulation tools, and field programmable gate array architectures.

4. Learning Approach

Approach : Combination of Expository - inquiry and colaborative
Method : Discussion, question answer, sample problem, group work
Software : Digital Designer (http://www.digitalcircuitdesign.com)
Student Task : Home work, presentation
Media : LCD projector, Teaching Aids (components), Simulation SW, film.

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5. Evaluation

a) Absence maximum : 25%
b) Quiz & participation : 10 points
c) Projects : 30 points
d) Final Examination : 60 points

Total : 100 points

6. Contents/ Topics of Lecturing:

Week	Content/ Topics of Lecturing	Text Book Chapter	Remark
1	**Introduction** The Game Plan, The Art of Managing Complexity, The Digital Abstraction, Number Systems, Logic Gates, Beneath the Digital Abstraction	Ch1	
2-3	**Combinational Logic Design:** Boolean Equations, Boolean Algebra, From Logic to Gates, Karnaugh Maps, Combinational Building Block	Ch2	Introduction Verilog
4-5	**Sequential Logic Design:** Latches and Flip-Flop, Synchronous Logic design (Synchronous Sequential Circuits, Synchronous and Asynchronous Circuits)	Ch3	
6-7	**Sequential Logic Design - State Machine and Counters:** Finite State Machines (Design Example, State Encodings , Moore and Mealy Machines, Factoring State), Timing of Sequential Logic	Ch3	
7	**Digital Building Block:** Arithmetic Circuits, Number Systems	Ch5	
8	**Mid Term Break**		
9	**Digital Building Block:** Sequential building block, Memory & logic arrays	Ch5	
10-12	**High Level Design w/Verilog** Modeling with Continuous Assignments, Modeling with Always Blocks	Handout	Verilog
13-14	**High Level Design w/Verilog** Finite State Machines, Bad Circuit Examples	Handout	Verilog
15	**Final Examination**		

7. Book Reference:

a) **Main Text Book:** *"Digital Design and Computer Architecture- ARM Edition*, **Author:** David Money Harris and Sarah L. Harris, **Publisher**: Morgan Kaufmann, 2007, ISBN 10: 0-12-370497-9

b) Structural Design with Verilog, David Harris, hand out, Harvey Mud Colledge, 2000

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